Current Listing of Claims

Kindly replace any previous listing of claims with the present listing of claims.

1. (currently amended) A digital signal processor comprising:

an instruction memory , a central arithmetic unit, a register, a controller, and input/output devices;

characterized in that

the instruction memory is arranged to include logical operations, time performance constraints and events ~~event~~;

the controller is arranged to suspend further processing of time performance constraints after initiating operations in an event control unit and resume processing when advised by the event control unit; and

the event control unit is arranged to recognize an event that initiates processing by the event control unit, wherein the event is an input signal and to control processing to be carried out as a consequence of the event while fulfilling the time performance constraints, wherein a pulse package held in the event control unit includes an event operand operable to identify the input signal to initiate processing by the event control unit and a delay operand that defines a stop condition for a counter in the event control unit ~~and~~

~~the controller is arranged to resume processing when advised by the event control unit~~.

2. (currently amended) A digital signal processor in accordance with claim 1, wherein the event is ~~recognized in a detector and introduced as a level transition to the~~ detected by the event

control unit.

3. (currently amended) A digital signal processor in accordance with claim 2, wherein the event control unit ~~detector~~ is arranged to detect input signals ~~by determining the energy level in the signal~~.

4. (currently amended) A digital signal processor in accordance with claim 2, wherein a further event is recognized as a completion of the processing carried out as a consequence of the ~~previous~~ event.

5. (currently amended) A digital signal processor in accordance with claim 1, wherein the event is recognized as a completion of the processing carried out as a consequence of ~~the~~ a previous event.

6. (currently amended) A digital signal processor in accordance with claim 1, wherein the event control unit includes ~~including~~ a signal memory arranged to store and extract data under control of the event control unit.

7. (currently amended) A digital signal processor in accordance with claim 6, wherein the signal memory is a vector memory ~~with low granularity and where the granularity determines a split between a high-resolution part and a low-resolution part of the time performance constraints~~.

8. (canceled) ~~A digital signal processor in accordance with claim 7, wherein the event control unit is arranged to process the low-resolution part.~~

9. (canceled) ~~A digital signal processor in accordance with claim 7, wherein the high-resolution part is processed during memory access to the signal memory by delaying the access to the signal memory a period of time corresponding to the high-resolution part..~~

10. (previously presented) A digital signal processor in accordance with claim 1, including two or more event control units arranged to work independently from each other.